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Question Paper Code : 30117

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Computer Science and Engineering

CS 3351 — DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design/Computer Science and Engineering (Artificial Intelligence and Machine Learning)/Computer Science and Engineering (Cyber Security)/Computer and Communication Engineering/Artificial Intelligence and Data Science/Computer Science and Business Systems/Information Technology)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Construct Half-adder and full adder circuits.
2. Evaluate the logic circuit of 2 bit comparator.
3. Distinguish sequential logic with combinational logic.
4. Give the excitation table of JK flip flop.
5. Draw the block diagram of Von-Neumann architecture.
6. List the types of addressing modes.
7. What do you mean by pipelining? List its types.
8. Differentiate data hazards and control hazards.
9. Why do we need cache memory?
10. Which signal is used to notify the processor that the transfer is completed? Define.

PART B — (5 × 13 = 65 marks)

11. (a) (i) How will you design a full adder using two half adders. (7)
(ii) Simplify the function using multiplexer $f = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (6)
- Or
- (b) (i) Demonstrate 4 bit magnitude comparator with three outputs $A > B$, $A = B$, $A < B$. (7)
(ii) Build a 4 bit priority encoder using gates. (6)

12. (a) (i) Realize D flip flop using SR flip flop. (7)
(ii) Construct a 4 bit down counter using logic gates. (6)

Or

- (b) Give the analysis and design of clocked sequential circuits.
13. (a) (i) Explain about functional units in digital computer. (7)
(ii) Discuss about instruction cycle. (6)

Or

- (b) (i) Explain about encoding in assembly language and types of instructions. (7)
(ii) Discuss the interaction between assembly language and high level language. (6)
14. (a) An instruction pipeline has five stages where each stage takes 2 nanoseconds and all instructions use all five stages, branch instructions are not overlapped (i.e.) the instruction after the branch is not fetched till the branch instruction is completed. Under ideal condition. Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instructions. Ignore the fact that some branch instructions may be conditional.

Or

- (b) (i) What is hazard? Give hazard free realization for the following Boolean function $F(A, B, C, D) = \Sigma m(1, 5, 6, 7)$ using AND-OR gate network. (10)
(ii) Define essential hazards. (3)
15. (a) (i) Explain in detail about DMA operation. (7)
(ii) Give the modes of DMA transfer. (6)

Or

- (b) Elucidate interconnection standards.

PART C — (1 × 15 = 15 marks)

16. (a) Explain the functions with the state diagram and characteristic equation of T, D and JK flip flop. Compare and Contrast.

Or

- (b) Implement the following Boolean function using 8 x 1 multiplexer. Considering D as the input and A, B, C as selection lines $f(A, B, C, D) = AB' + BD + B'CD'$.
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