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Question Paper Code : 40980

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024.

Third Semester

Electronics and Communication Engineering

EC 3353 — ELECTRONIC DEVICES AND CIRCUITS

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the voltage current equation of PN junction diode.
2. Draw the circuit of half wave rectifier.
3. What is an operating point in an amplifier design?
4. Why gain of an amplifier reduces at high frequencies?
5. What is common mode gain?
6. Differentiate single and double tuned amplifier.
7. Define Barkhausen criterion for oscillations.
8. List the advantages of negative feedback.
9. Compare Class A and Class B power amplifier.
10. List the three basic types of DC/DC Converter.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the working of bridge type full of rectifier with neat sinusoidal waveform at the input and sketch the output waveform. Determine the V_{dc} and PIV .

Or

- (b) Explain the following characteristics of a silicon BJT transistor in the common emitter configuration.

- (i) Collector characteristics (7)

- (ii) Base characteristics (6)

12. (a) Derive the voltage gain, input impedance and output impedance for the small signal model of CE Voltage divider configuration. Also mention the phase relation between the input and output.

Or

- (b) Derive the voltage gain, input impedance and output impedance for the small signal model of E MOSFET CS - Voltage divider configuration.
13. (a) For the network of Fig. 1 [Fig. 1: n-channel JFET amplifier. Source V_s with 1 kohm series resistor coupled through 0.1 microF to the gate (V_1 , input impedance Z_i); 1 Mohm from gate to ground; drain to 18 V through 3 kohm; drain coupled through 4.7 microF to output V_o across a 3.9 kohm load; source to ground through 1.2 kohm bypassed by 10 microF. $I_{DSS} = 6$ mA, $V_p = -6$ V, $r_d = \text{infinity ohm}$. $C_{Wi} = 3$ pF, $C_{Wo} = 5$ pF, $C_{gd} = 4$ pF, $C_{gs} = 6$ pF, $C_{ds} = 1$ pF.]
- (i) Determine g_{m0} and g_m . (4)
- (ii) Find A_v and A_{vs} in the mid-frequency range. (3)
- (iii) Determine f_{Hi} and f_{Ho} . (3)
- (iv) What is the gain-bandwidth product of the amplifier? (3)

Or

- (b) For the cascode amplifier of Fig. 2. [Fig. 2: BJT cascode amplifier, $V_{CC} = 22$ V. Bias divider $R_{B1} = 8.2$ kohm, $R_{B2} = 4.7$ kohm, $R_{B3} = 3.3$ kohm from V_{CC} to ground; base of Q_2 ($\beta_2 = 120$) at the R_{B1} - R_{B2} junction, bypassed to ground by $C_1 = 10$ microF; base of Q_1 ($\beta_1 = 60$) at the R_{B2} - R_{B3} junction, input V_i through $C_s = 5$ microF. Q_2 collector to V_{CC} through $R_C = 2.2$ kohm, output V_o through $C = 5$ microF; Q_2 emitter to Q_1 collector; Q_1 emitter to ground through $R_E = 1.1$ kohm bypassed by $C_E = 20$ microF.] Determine
- (i) The base and collector currents of each transistor.
- (ii) The voltages V_{B1} , V_{B2} , V_{E1} , V_{C1} , V_{E2} and V_{C2} .
14. (a) Derive the input impedance, output impedance and voltage gain of voltage series feedback network using forward gain block A and feedback gain block beta.

Or

- (b) Explain the working of FET Colpitts oscillator. Also derive its frequency of oscillation.
15. (a) Explain the working of series fed class A large signal amplifier using a simple fixed bias circuit and derive the maximum efficiency.

Or

- (b) With suitable circuit diagram, elucidate the working of Buck Boost Converter.

PART C — (1 × 15 = 15 marks)

16. (a) [Fig. 3: 20 V source feeding series resistor $R_C = 220 \text{ ohm}$ (current I_R) into a Zener diode ($V_Z = 10 \text{ V}$, $P_{Z\max} = 400 \text{ mW}$, current I_Z) in parallel with load R_L (current I_L , voltage V_L).]
- (i) Determine V_L , I_L , I_Z and I_R for the network in Fig 3 of if $R_L = 180 \text{ ohm}$. (5)
 - (ii) Determine V_L , I_L , I_Z and I_R for the network of if $R_L = 470 \text{ ohm}$. (5)
 - (iii) Determine the value of R_L that will establish maximum power conditions for the Zener diode. (3)
 - (iv) Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state. (2)

Or

- (b) A buck boost converter operating at 20 kHz is shown in Fig. 4. The Output capacitor C is sufficiently large to ensure a ripple-free output voltage. The input voltage V_{in} is 15 V. The converter is supplying a load of 10 W. If the output voltage is required to be 10 V, find the duty ratio (D) of the switch. [Fig. 4: buck-boost converter: 15 V source, switch S , 50 microH inductor to ground, diode D , 390 microF output capacitor in parallel with load R across which the output is 10 V (inverted polarity).]